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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,598	02/10/2004	Po Jen Cheng	4459-090A	8879

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EXAMINER	
HOLLINGTON, JERMELE M	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,598	CHENG ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-11,13,15-17,19-22 and 24* is/are rejected.

7)☒ Claim(s) *12, 14, 18, 23 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 6-8 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 6-9, 15-16, and 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Field (6535005).

Regarding claim 6, Field discloses [see Figs. 1, 4 and 9] a test assembly (system 20) for an integrated circuit package, the test assembly (20) comprising: a package substrate (module 24) having a plurality of first contact pads (module contacts 82 shown in Fig. 4) [see also col. 8, lines 26-29] adapted for receiving solder bumps (solder balls 40) and a plurality of first conductors (conductive material 84) connecting selected pairs of said first contact pads (contacts 82 see Fig. 4); and a test board (printed circuit board 22) having a plurality of second contact pads (contact pads 152 shown in Fig. 9), a pair of major test pads (part of interface location 30), a plurality of minor test pads (part of interface location 30) connected to selected ones of said second contact pads (152), and a plurality of second conductors (conductive material 154) connecting selected

pairs of the second contact pads (152), wherein all of the second contact pads (152) are divided into a plurality of groups such that all of the second contact pads (152) in the same group are arranged in a line [horizontal line], wherein, when the package substrate (24) is mounted on the test board (22) with each of said solder bumps (40) soldered to one of the first contact pads (82) and one of the second contact pads (152), all of the pairs of connected second contact pads (152) and the corresponding pairs of connected first contact pads (82) form a conductive path that passes through all of the solder bumps (40), each of said groups of connected second contact pads (152) and the corresponding connected first contact pads (82) form a closed circuit through all of the solder bumps (40) there between when said major test pads (part of interface location 30) are probed, and when one pair of the minor test pads (part of interface location 30) is probe, only one of said groups of the second contact pads (152) and the corresponding connected first contact pads (82) form another closed circuit through all of the solder bumps (40) there between.

Regarding claim 7, Field discloses all of the second contact pads (152) belong to the closed circuit when the major test pads (interface location 30) are probed.

Regarding claim 8, Field discloses the package substrate (24) is a ball grid array substrate [see col. 12, lines 40-44].

Regarding claim 9, Field discloses wherein all of the second contact pads (152) in the same group are arranged in a straight line (horizontal straight line).

Regarding claim 15, Field discloses a test board (printed circuit board 22) for testing an integrated circuit package, the test board comprising: a plurality of contact pads (contact pads 152 shown in Fig. 9), a pair of major test pads (part of interface location 30) and a plurality of minor test pads (part of interface location 30) connected to selected ones of said second contact

pads (152), and a plurality of conductors (conductive material 154) connecting selected pairs of the second contact pads (152), wherein the contact pads (152) are divided into a plurality of groups such that all of the contact pads (152) and all of the associated conductors (154)in the same group are arranged in a line [horizontal line], and the contact pads (152) at the ends of said straight line are connected to one pair of said minor test pads (30), respectively.

Regarding claim16, Field discloses wherein the straight lines along which the contact pads (152) of some of said groups are arranged are parallel with each other.

Regarding claim 19, Field discloses [see Figs. 1, 4 and 9] a test assembly (system 20) for an integrated circuit package, the test assembly (20) comprising: a package substrate (module 24) having a plurality of first contact pads (module contacts 82 shown in Fig. 4) [see also col. 8, lines 26-29] adapted for receiving solder bumps (solder balls 40) and a plurality of first conductors (conductive material 84) each connecting one pair of said first contact pads (contacts 82 see Fig. 4) to define a first circuit portion; and a test board (printed circuit board 22) having a plurality of second contact pads (contact pads 152 shown in Fig. 9) and a plurality of second conductors (conductive material 154) each connecting one pair of the second contact pads (152) to define a first circuit portion, the test board (22) further comprising a pair of major test pads (part of interface location 30) and a plurality of minor test pads (part of interface location 30) connected to selected ones of said second contact pads (152), wherein the second contact pads (152) are divided into a plurality of groups such that all of the contact pads (152) and all of the associated second conductors (154) in the same group are arranged in a line [horizontal line], and the second contact pads (152) at the ends of said straight line are connected to one pair of said minor test pads (30), respectively; and wherein, when the package substrate (24) is mounted on the test

board (22) with each of said solder bumps (40) soldered to one of the first contact pads (82) and one of the second contact pads (152), the first and second circuit portions will be connected to define a conductive path that passes through all of the solder bumps (40) which are connected in series in said conductive path by said first (82) and second (152) pads and conductors (84).

Regarding claim 20, Field discloses wherein when one pair of the minor test pads (part of interface location 30) connected to the second contact pads (152) at the end of the straight line of one of said groups is probed only said group of the second contact pads (152) and the corresponding connected first contact pads (82) form a closed circuit through all of the solder bumps (40) there between.

Regarding claim 21, Field discloses when one pair of the minor test pads (part of interface location 30) connected to the second contact pads (152) at the end of the straight line of one of said groups is probed, said group of the second contact pads (152) and the corresponding connected first contact pads (82) form a closed circuit through all of the solder bumps (40) there between and wherein all of the first (84) and second (154) conductors which belong to said closed circuit extend along said straight line.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 10-11, 13, 17, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fields (6535005).

Regarding claims 10 and 17, Fields disclose (see Figs. 1, 4 and 9) an IC package substrate (module 24) having a plurality of first contact pads (module contacts 82 shown in Fig. 4) [see also col. 8, lines 26-29] and a plurality of first conductors (conductive material 84) selected ones of first contact pads [see Fig. 4] to define a first circuit portion, and a test board (circuit board 22) having a plurality of second contact pads (contacts 152 shown in Fig. 9) and a plurality of second conductors (conductive material 154). However, he does not disclose the straight line is parallel to an edge of the test board as claimed. It is well known to have a straight line parallel to the test board where needed (see MPEP 2144.04 *In re Seid*, 161 F.2d 229, 73 USPQ 431 (CCPA 1947)). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have a straight line parallel to the test board edge since the straight line, which is an aesthetic design change with no mechanical function, would provide support in a selective manner to each individual user in arranging contact pads with the edge of the test board.

Regarding claims 11, 13, 22 and 24, Fields disclose (see Figs. 1, 4 and 9) an IC package substrate (module 24) having a plurality of first contact pads (module contacts 82 shown in Fig.

4) [see also col. 8, lines 26-29] and a plurality of first conductors (conductive material 84) selected ones of first contact pads [see Fig. 4] to define a first circuit portion, and a test board (circuit board 22) having a plurality of second contact pads (contacts 152 shown in Fig. 9) and a plurality of second conductors (conductive material 154). However, he does not disclose at least one spiral section extending around the test board as claimed. It is well known to have spiral section extending around the test board where needed (see MPEP 2144.04 *In re Seid*, 161 F.2d 229, 73 USPQ 431 (CCPA 1947)). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have spiral section extending around the test board central area since the spiral section, which is an aesthetic design change with no mechanical function, would provide support in a selective manner to each individual user in using conductive path as a closed circuit on the test board.

Conclusion

7. Claims 12, 14, 18, 23 and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: regarding claims 12, 14, 23 and 25 in the examiner's opinion, it would not have been obvious to a person of ordinary skill in the art to have, in the prior art, a conductive path with two spiral sections connected to test pads so that the entire conductive path belong in a closed circuit.

Regarding claim 18, the primary reason for the allowance for the allowance of the claim is due to the straight lines along which the contact pads of said groups are arranged are divided into four groups.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on (517) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Patent Examiner
Art Unit 2829

JMH
November 2, 2004